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PATENT ABSTRACTS OF JAPAN

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(71)Applicant : NEC CORP

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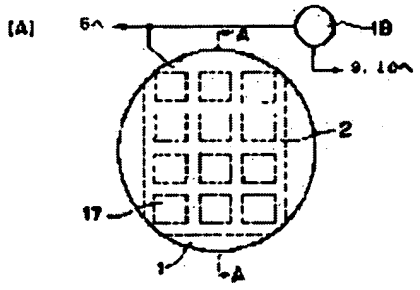
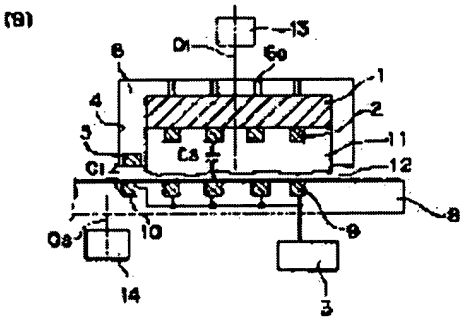
(54) POLISHING AMOUNT CONTROL DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a polishing amount control device whereby a local residual film thickness of a wafer can be measured, so as to prevent a bad influence from being given to a characteristic of a semiconductor chip by measuring applied voltage.

SOLUTION: Opposed to an electrode 2 in a dicing area formed in a wafer 1, a measuring electrode 9 is divisionally arranged in a polishing pad 8. In a wafer hold means 6 in a side of the wafer 1, a correction electrode 5 is provided, on the other hand, a correcting measuring electrode 10 is left as provided in a position opposed to the correction electrode 5 of the polishing pad 8. In this condition, polishing is performed, and a static capacity between the electrode 2 and the measuring electrode 9 is obtained. In accordance with a of this measured capacity value, pressure of air is applied from a local pressure hole 6a, an inter-layer insulating film 11 of the wafer is pressed to a side of the pad 8, and polishing is performed in this pressed condition.





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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the amount control unit of polishes which is applied to the amount control unit of polishes, especially controls the amount of polishes of the front face of a semi-conductor wafer.
[0002]
[Description of the Prior Art] In the manufacture process of a semi-conductor wafer, flattening of the front face of this semi-conductor wafer may be ground and carried out. The check of the degree of this flattening is performed by measuring the residual film thickness on the front face of a wafer. Drawing 5 is the block diagram of an example of a means to measure the conventional residual film thickness (for example, JP,4-357851,A).
[0003] It has the dielectric layer 102 by which the conventional residual membrane measurement means was formed in the inferior surface of tongue of a wafer 101 and this wafer 101 as shown in drawing 5 , the polish plate 103 which grinds a wafer 101 while rotating, the slurry 104 which is an abrasive material at the time of grinding a wafer, the amplifier 105 which shifts 180 degrees of phases of the input voltage for measurement, and the measurement section 106 grade which computes thickness from the measured displacement current. Two electrodes 103a and 103b insulated mutually are formed in said polish plate 103.
[0004] In this condition, to the measurement electrical potential difference impressed to electrode (protection electrode) 103b of another side, about 180 degrees, the measurement electrical potential difference impressed to one electrode (measuring electrode) 103a shifts a phase, and is impressed. And a drive current is supplied to protection electrode 103b with measuring-electrode 103a and a bootstrap system, and the measurement section 106 keeps the displacement current constant so that the amplitude of driver voltage may be proportional to dielectric layer thickness. And residual film thickness is measured by measuring the electrical potential difference outputted from the measurement section 106.

[0005]
[The technical problem which invention makes solution ******] However, there was the following trouble in the conventional measurement means. That is, the average of the thickness of the whole wafer will be detected with the conventional measurement means. therefore -- the time of diameter[of macrostomia]-izing a wafer -- being partial (local) -- although the amounts of residual membranes differ, and this partial amount of residual membranes is measured, it cannot do. Moreover, although chip area and dicing area are formed in a wafer, since the electrical potential difference for residual-film-thickness measurement is impressed also to chip area and the electric field by this electrical potential difference occur, it will have a bad influence on the property of a semiconductor chip.
[0006] Then, the local residual film thickness of a wafer of the purpose of this invention is measurable, and it is offering the amount control unit of polishes it was made not to have a bad influence on the property of a semiconductor chip with the applied voltage for measurement.
[0007]
[Means for Solving the Problem] In order to solve said technical problem invention according to claim 1 The ground object with which the 1st electrode was prepared along the polished surface, and the scouring pad with which the 2nd electrode was prepared in the location which opposite arrangement is carried out at this ground object, and counters said 1st electrode, It is characterized by having an electrical-potential-difference impression means to impress an electrical potential difference between said 1st electrode and 2nd electrode, and a volumetry means to measure the capacity between said 1st electrode and 2nd electrode. Moreover, invention according to claim 4 is characterized by having a press means to turn the part of the request in said ground object to said scouring pad, and to press it. Moreover, said ground object of invention according to claim 6 is a semi-conductor wafer, and it is characterized by forming said 1st electrode in dicing area parts other than the chip area formed in this semi-conductor wafer.
[0008] Are in the condition carried out in this way, for example, divide the 2nd electrode of a scouring pad, the 1st

electrode is made to counter, and the capacity of each part corresponding to this 2nd electrode is measured. The part which carries out electrical-potential-difference impression in this case is dicing area. And according to the size of this measured capacity value, a ground object is pushed against a scouring pad side with a press means, and it grinds in this condition of having pushed. If it does in this way, since electrical-potential-difference impression will be carried out in dicing area, it becomes possible not to have a bad influence on the property of a semiconductor chip, and to control partially the thickness of the semi-conductor wafer of the diameter of macrostomia.
[0009]
[Embodiment of the Invention] Hereafter, this invention is explained based on the example of an operation gestalt of illustration. Drawing 1 and drawing 2 are drawings showing this example of an operation gestalt, and the sectional view where drawing 1 (A) meets the top view of a wafer, and drawing 1 (B) meets an A-A line, and drawing 2 are the top views showing the physical relationship of a scouring pad and a wafer.
[0010] As shown in drawing 1 and drawing 2 , it is the object section in which an interlayer insulation film 11 is formed in the inferior-surface-of-tongue side of the circular wafer 1 at one, and the inferior surface of tongue of this interlayer insulation film 11 grinds [drawing 1 (A) and (B)]. Two or more LSI chip area 17 is formed in a wafer 1 of the dicing area formed in the shape of a matrix, and the electrode 2 is formed in this dicing area. One pole of the drive power source 18 for measurement is connected to this electrode 2. A wafer 1 is held so that the perimeter of this wafer may be surrounded by the wafer attachment component 6, and partial pressurization hole 6a which impresses the pneumatic pressure supplied from the pneumatic pressure generator which is not illustrated is drilled in this attachment component 6 corresponding to the direction of a train of the electrode 2 arranged in the shape of a matrix. The rotation drive of the wafer attachment component 6 is carried out by the rotation means which is not illustrated around the medial axis O1 (refer to drawing 1 (B) and drawing 2) of a wafer 1, with the wafer 1 held. Angle of rotation of a wafer 1 is a medial axis O1. It is detected by the wafer angle-of-rotation detector 13 linked directly.
[0011] Moreover, it is a medial axis O8 by rotation means by which a scouring pad 8 is arranged under the wafer 1, and this pad 8 is not illustrated. A rotation drive is carried out around. That is, a wafer 1 and a scouring pad 8 rotate in the state of the eccentricity from which the center of rotation differed (refer to drawing 2). Angle of rotation of a scouring pad 8 is a medial axis O1. It is detected by the scouring pad angle-of-rotation detector 14 linked directly. Between the interlayer insulation film 11 of a wafer, and a scouring pad 8, the non-conductive slurry (abrasive material) 12 is supplied.
[0012] The wafer attachment component 6 is equipped with the retainer 4 held firmly so that there may be no dedropping a wafer 1, it is the interior of this retainer 4, and the proofreading electrode 5 is embedded at the opposed face with a scouring pad 8. This proofreading electrode 5 is connected to one pole of said drive power source 18. Moreover, in the interior of the top-face side of a scouring pad 8, the measuring electrode 10 for proofreading and the measuring electrode 9 are embedded. The measuring electrode 9 and the measuring electrode 10 for proofreading are connected to the pole of another side of said drive power source 18.
[0013] And as shown in drawing 2 , there is one measuring electrode 10 for proofreading, and the electrode 9 for measurement counters the electrode 2 formed in the dicing area of a wafer 1, and are prepared. [two or more] There is also a proofreading electrode 5 prepared in the retainer 4 of a wafer 1.
[0014] Next, actuation of this example of an operation gestalt is explained, referring to drawing 3 and drawing 4 .
(1) After the measurement interlayer insulation film 11 and scouring pad 8 of residual film thickness have contacted, the rotation drive of a wafer 1 and the scouring pad 11 is carried out in the same direction by the rotation means which is not illustrated, and polish is performed. And in measuring the residual film thickness of an interlayer insulation film 11 during polish, it checks that the relative rotation location of the proofreading electrode 5 prepared in the wafer 1 and the measuring electrode 10 for proofreading prepared in the scouring pad 8 has been in agreement with the wafer angle-of-rotation detector 13 and the scouring pad angle-of-rotation detector 14.
[0015] In the state of coincidence of this relative rotation location, the electrostatic capacity C1 (refer to drawing 3) by the slurry 12 which intervened between the proofreading electrode 5 and the measuring electrode 10 for proofreading is measured with the electrostatic-capacity measuring instrument 3. Electrostatic capacity C3 according to the electrode 2, the measuring electrode 9, and slurry 12 of a wafer to coincidence It measures with the electrostatic-capacity measuring instrument 3. Said electrostatic capacity C1 It is the electrostatic capacity used as criteria, even if a wafer 1 is ground, it is eternal, and it is said electrostatic capacity C3. It changes by polish.
[0016] and said electrostatic capacity C3 from -- electrostatic capacity C1 Deducted electrostatic capacity C2 It becomes the capacity resulting from the thickness (residual film thickness) of an interlayer insulation film 11. This electrostatic capacity C2 It is based and asks for residual film thickness. In addition, electrostatic-capacity value C2 What is necessary is just to prepare the relation with residual film thickness as a table beforehand according to the quality of the material of an interlayer insulation film, the quality of the material of a slurry, etc. If measurement of the above residual film thickness is performed to all the measuring electrodes 9 in a scouring pad 8, it will become possible to detect irregularity

with a partial (local) wafer front face.
[0017] (2) As partial pressurization showed to polish drawing 4 (A), suppose that irregularity is formed in the inferior surface of tongue of an interlayer insulation film 11. The residual film thickness of this insulator layer 11 presupposes that they are "a, b, c, d" sequentially from the left, and presupposes that there is relation of c=d>a>b. In this case, arrow-head p1 -p4 shown in drawing (A) from the partial pressurization hole six a1 to 6a4 of the part corresponding to a-d Air pressurization of the magnitude corresponding to die length is performed, and it is p3 =p4 >p1 >p2. It grinds with a scouring pad 8 in the state of pressurization. If it does in this way, since the amount of polishes can be adjusted according to residual film thickness, it becomes possible to carry out flattening through the interlayer insulation film 11 whole.
[0018] In addition, although this example of an operation gestalt explained the case of a semi-conductor wafer as a ground object, of course, this invention is applicable also to the object of which flat [other] are required.
[0019]
[Effect of the Invention] Since the amount of polishes according to the part of each [the condition of having divided the ground object (semi-conductor wafer)] is controllable according to this invention as explained above, even if it is the semi-conductor wafer of the diameter of macrostomia, flattening of the whole front face can be carried out. Moreover, since the electrical potential difference for measurement is impressed to the dicing area of a semi-conductor wafer, it does not have a bad influence on the property of a semiconductor chip.

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The amount control unit of polishes which opposite arrangement is carried out at the ground object with which the 1st electrode was prepared along the polished surface, and this ground object, and is characterized by to have an electrical-potential-difference impression means impress an electrical potential difference between the scouring pad with which the 2nd electrode was prepared in the location which counters said 1st electrode, and said 1st electrode and 2nd electrode, and a volumetry means measure the capacity between said 1st electrode and 2nd electrode.
[Claim 2] The amount control unit of polishes according to claim 1 characterized by supplying an abrasive material between said ground objects and scouring pads.
[Claim 3] The amount control unit of polishes given in either claim 1 characterized by having the reference electrode prepared in the opposed face with said scouring pad of a maintenance means to hold said ground object, and the reference electrode for measurement prepared in the location which counters said reference electrode of said scouring pad, or claim 2.
[Claim 4] The amount control unit of polishes according to claim 1 to 3 characterized by having a press means to turn the part of the request in said ground object to said scouring pad, and to press it.
[Claim 5] Said press means is the amount control unit of polishes according to claim 4 characterized by being the air pressure supply means formed in said maintenance means.
[Claim 6] It is the amount control unit of polishes according to claim 1 to 5 characterized by for said ground object being a semi-conductor wafer, and forming said 1st electrode in dicing area parts other than the chip area formed in this semi-conductor wafer.
[Claim 7] The amount control unit of polishes according to claim 1 to 6 characterized by measuring the capacity of each part between the 1st electrode formed in said dicing area, and two or more 2nd electrodes formed in said scouring pad with said volumetry means, and pressing this each part with said press means according to the measurement result of each part of said.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the example of an operation gestalt of this invention, and is the sectional view where (A) meets the top view of a wafer and (B) meets an A-A line.
[Drawing 2] It is the top view showing the electrode disposition of the scouring pad of this example of an operation gestalt.
[Drawing 3] It is drawing showing the inter-electrode electrostatic capacity at the time of grinding in this example of an operation gestalt.
[Drawing 4] It is drawing showing the partial pressurization at the time of grinding in this example of an operation gestalt, and (A) is a sectional view and (B) is a top view.
[Drawing 5] It is the outline block diagram of the conventional amount control unit of polishes.
[Description of Notations]
1 Wafer (Ground Object)
2 Electrode (1st Electrode)
3 Electrostatic-Capacity Measuring Instrument (Volumetry Means)
4 Retainer
5 Proofreading Electrode (Reference Electrode)
6 Wafer Attachment Component
6a Partial pressurization hole (a press means, air pressure supply means)
8 Scouring Pad
9 Measuring Electrode (2nd Electrode)
10 Measuring Electrode for Proofreading (Reference Electrode for Measurement)
11 Interlayer Insulation Film (Ground Object)
12 Slurry (Abrasive Material)
17 Chip Area

[Translation done.]

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			Ｗ
Ｈ０１Ｌ　21/304	３２１	Ｈ０１Ｌ　21/304	３２１Ｅ

審査請求　有　　請求項の数７　ＦＤ　（全５頁）

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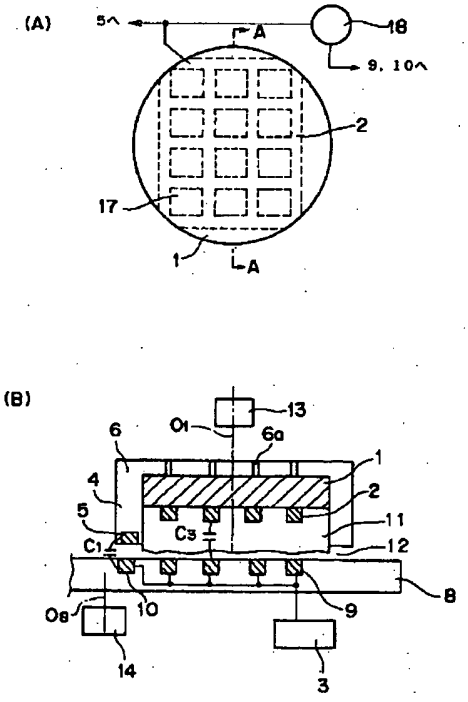
(54)【発明の名称】　研磨量制御装置

(57)【要約】

【課題】　ウェハの局所的な残膜厚が測定可能であり、測定用印加電圧により半導体チップの特性に悪影響を与えないようにした研磨量制御装置を提供する。

【解決手段】　ウェハ１に形成されたダイシングエリアの電極２に対向して、研磨パッド８に測定電極９を分割配置する。また、ウェハ１側のウェハ保持手段６に校正電極５を設け、一方研磨パッド８の前記校正電極５に対向した位置に校正用測定電極１０を設けておく。この状態で研磨を行い、電極２と測定電極９との間の静電容量を求める。そして、この測定容量値の大小に応じて局所加圧孔６ａから空気加圧してウェハの層間絶縁膜を研磨パッド側に押しつけ、この押しつけた状態で研磨を行う。



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【特許請求の範囲】

【請求項１】　研磨面に沿って第１電極が設けられた被研磨物と、

該被研磨物に対向配置され、前記第１電極に対向する位置に第２電極が設けられた研磨バッドと、

前記第１電極と第２電極との間に電圧を印加する電圧印加手段と、

前記第１電極と第２電極との間の容量を測定する容量測定手段とを備えたことを特徴とする研磨量制御装置。

【請求項２】　前記被研磨物と研磨バッドとの間に研磨剤を供給するようにしたことを特徴とする請求項１記載の研磨量制御装置。

【請求項３】　前記被研磨物を保持する保持手段の、前記研磨バッドとの対向面に設けられた基準電極と、

前記研磨バッドの、前記基準電極に対向する位置に設けられた測定用基準電極とを備えたことを特徴とする請求項１または請求項２のいずれかに記載の研磨量制御装置。

【請求項４】　前記被研磨物における所望の箇所を、前記研磨バッドに向けて押圧する押圧手段を備えたことを特徴とする請求項１乃至請求項３のいずれかに記載の研磨量制御装置。

【請求項５】　前記押圧手段は前記保持手段に設けられた空気圧供給手段であることを特徴とする請求項４記載の研磨量制御装置。

【請求項６】　前記被研磨物は半導体ウェハであり、

前記第１電極は該半導体ウェハに形成されたチップエリア以外のダイシングエリア部分に形成されたことを特徴とする請求項１乃至請求項５のいずれかに記載の研磨量制御装置。

【請求項７】　前記ダイシングエリアに形成された第１電極と、前記研磨バッドに形成された複数の第２電極との間の個々の箇所の容量を前記容量測定手段で測定し、前記個々の箇所の測定結果に応じて前記押圧手段により該個々の箇所を押圧するようにしたことを特徴とする請求項１乃至請求項６のいずれかに記載の研磨量制御装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、研磨量制御装置に係り、特に半導体ウェハの表面の研磨量を制御する研磨量制御装置に関する。

【０００２】

【従来の技術】半導体ウェハの製造過程においては、該半導体ウェハの表面を研磨し平坦化する場合がある。この平坦化の度合の確認は、ウェハ表面の残膜厚を測定することにより行っている。図５は従来の残膜厚を測定する手段の一例のブロック図である（例えば、特開平４－３５７８５１号公報）。

【０００３】図５に示すように、従来の残膜測定手段

2

は、ウェハ１０１と、該ウェハ１０１の下面に形成された誘電体層１０２と、回転しながらウェハ１０１を研磨する研磨プレート１０３と、ウェハを研磨する際の研磨剤であるスラリ１０４と、測定用の入力電圧の位相を１８０°ずらす増幅器１０５と、測定した変位電流から膜厚を算出する計測部１０６等を備えている。前記研磨プレート１０３には相互に絶縁された２つの電極１０３ａ，１０３ｂが形成されている。

【０００４】この状態で、一方の電極（測定電極）１０３ａに印加される測定電圧は、他方の電極（保護電極）１０３ｂに印加される測定電圧に対して１８０°位相をずらして印加される。そして、測定電極１０３ａとブートストラップ方式で保護電極１０３ｂに駆動電流を供給し、計測部１０６は、駆動電圧の振幅が誘電体層の厚さに比例するように、変位電流を一定に保つ。そして、計測部１０６から出力される電圧を測定することにより残膜厚を測定を行っている。

【０００５】

【発明が解決しょうとする課題】しかしながら、従来の測定手段には次の問題点があった。即ち、従来の測定手段ではウェハ全体の厚さの平均値を検出することになってしまう。従って、ウェハを大口径化したときには部分的（局所的）に残膜量が異なるが、この部分的な残膜量を測定するができない。また、ウェハにはチップエリアとダイシングエリアとが形成されるが、チップエリアにも残膜厚測定用の電圧を印加し、該電圧による電界が発生するので、半導体チップの特性に悪影響を与えてしまう。

【０００６】そこで、本発明の目的は、ウェハの局所的な残膜厚が測定可能であり、測定用印加電圧により半導体チップの特性に悪影響を与えないようにした研磨量制御装置を提供することである。

【０００７】

【課題を解決するための手段】前記課題を解決するために請求項１記載の発明は、研磨面に沿って第１電極が設けられた被研磨物と、該被研磨物に対向配置され、前記第１電極に対向する位置に第２電極が設けられた研磨バッドと、前記第１電極と第２電極との間に電圧を印加する電圧印加手段と、前記第１電極と第２電極との間の容量を測定する容量測定手段とを備えたことを特徴とする。また、請求項４記載の発明は、前記被研磨物における所望の箇所を、前記研磨バッドに向けて押圧する押圧手段を備えたことを特徴とする。また、請求項６記載の発明は、前記被研磨物は半導体ウェハであり、前記第１電極は該半導体ウェハに形成されたチップエリア以外のダイシングエリア部分に形成されたことを特徴とする。

【０００８】このようにした状態で、例えば研磨バッドの第２電極を分割して第１電極に対向させ、該第２電極に対応した個々の箇所の容量を測定する。この場合の電圧印加をする箇所はダイシングエリアである。そして、

この測定した容量値の大小に応じて押圧手段により被研磨物を研磨パッド側に押しつけ、この押しつけた状態で研磨を行う。このようにすれば、ダイシングエリアに電圧印加するので、半導体チップの特性に悪影響を及ぼすことがなく、また、大口径の半導体ウェハの厚みを部分的に制御することが可能となる。

【０００９】

【発明の実施の形態】以下、本発明を図示の実施形態例に基づいて説明する。図１，図２は本実施形態例を示す図であって、図１（Ａ）はウェハの平面図、図１（Ｂ）はＡ－Ａ線に沿う断面図、図２は研磨パッドとウェハの位置関係を示す平面図である。

【００１０】図１，図２に示すように、円形のウェハ１の下面側には層間絶縁膜１１が一体に形成され、該層間絶縁膜１１の下面が研磨をする対象部である〔図１（Ａ），（Ｂ）〕。ウェハ１にはマトリクス状に形成したダイシングエリアにより複数のＬＳＩチップエリア１７が形成され、該ダイシングエリアには電極２が形成されている。該電極２には測定用の駆動電源１８の一方の極が接続されている。ウェハ１はウェハ保持部材６により該ウェハの周囲を囲むように保持され、該保持部材６には図示しない空気圧発生装置から供給される空気圧を印加する局所加圧孔６ａが、マトリクス状に配置された電極２の列方向に対応して穿設されている。ウェハ保持部材６はウェハ１を保持したまま、図示しない回転手段によりウェハ１の中心軸Ｏ１（図１（Ｂ），図２参照）の回りに回転駆動される。ウェハ１の回転角度は、中心軸Ｏ１に直結したウェハ回転角度検出器１３により検出される。

【００１１】また、ウェハ１の下方には研磨パッド８が配置され、該パッド８は図示しない回転手段により中心軸Ｏ８の回りに回転駆動される。即ち、ウェハ１と研磨パッド８とは、回転中心の異なった偏芯状態で回転する（図２参照）。研磨パッド８の回転角度は、中心軸Ｏ１に直結した研磨パッド回転角度検出器１４により検出される。ウェハの層間絶縁膜１１と研磨パッド８との間には、非導電性のスラリ（研磨剤）１２が供給されるようになっている。

【００１２】ウェハ保持部材６はウェハ１を脱落しないように強固に保持するリテーナ４を備えており、該リテーナ４の内部であって、研磨パッド８との対向面には、校正電極５が埋め込まれている。該校正電極５は前記駆動電源１８の一方の極に接続されている。また、研磨パッド８の上面側の内部には校正用測定電極１０と測定電極９とが埋め込まれている。測定電極９と校正用測定電極１０とは前記駆動電源１８の他方の極に接続されている。

【００１３】そして、図２に示すように、校正用測定電極１０は１個であり、測定用電極９はウェハ１のダイシングエリアに形成された電極２に対向して、複数設けられている。ウェハ１のリテーナ４に設けられた校正電極５も１個である。

【００１４】次に本実施形態例の動作を、図３，図４を参照しつつ説明する。

（１）残膜厚の測定

層間絶縁膜１１と研磨パッド８とが当接した状態で、図示しない回転手段によりウェハ１と研磨パッド１１とが同一方向に回転駆動され、研磨が行われる。そして、研磨中において、層間絶縁膜１１の残膜厚を測定する場合には、ウェハ１に設けた校正電極５と研磨パッド８に設けた校正用測定電極１０との相対回転位置が一致したことを、ウェハ回転角度検出器１３と研磨パッド回転角度検出器１４とにより確認する。

【００１５】この相対回転位置の一致状態で、校正電極５と校正用測定電極１０との間に介在されたスラリ１２による静電容量Ｃ１（図３参照）を静電容量測定器３により測定する。同時に、ウェハの電極２と測定電極９とスラリ１２による静電容量Ｃ３を静電容量測定器３により測定する。前記静電容量Ｃ１は基準となる静電容量であり、ウェハ１が研磨されても不変であり、前記静電容量Ｃ３は研磨により変動する。

【００１６】そして、前記静電容量Ｃ３から静電容量Ｃ１を差し引いた静電容量Ｃ２が層間絶縁膜１１の厚さ（残膜厚）に起因する容量となる。この静電容量Ｃ２に基づいて残膜厚を求める。なお、静電容量値Ｃ２と残膜厚との関係は、層間絶縁膜の材質，スラリの材質等に応じて予めテーブルとして用意しておけばよい。以上のような残膜厚の測定を研磨パッド８内の全ての測定電極９に対して行なえば、ウェハ表面の部分的（局所的）な凹凸を検出することが可能となる。

【００１７】（２）局所加圧により研磨

図４（Ａ）に示したように、層間絶縁膜１１の下面に凹凸が形成されているとする。該絶縁膜１１の残膜厚は左から順に「ａ，ｂ，ｃ，ｄ」であるとし、ｃ＝ｄ＞ａ＞ｂの関係があるとする。この場合は、ａ～ｄに対応する部分の局所加圧孔６ａ1～６ａ4から、図（Ａ）に示す矢印ｐ１～ｐ４の長さに対応した大きさの空気加圧を行い、ｐ３＝ｐ４＞ｐ１＞ｐ２の加圧状態で研磨パッド８により研磨を行う。このようにすれば、残膜厚に応じて研磨量を加減することができるので、層間絶縁膜１１全体を通じて平坦化することが可能となる。

【００１８】なお、本実施形態例では被研磨物として半導体ウェハの場合を説明したが、その他の平坦さを要求される物にも本発明を適用できるのは勿論である。

【００１９】

【発明の効果】以上説明したように本発明によれば、被研磨物（半導体ウェハ）を分割した状態で個々の箇所に応じた研磨量を制御できるので、大口径の半導体ウェハであっても表面全体を平坦化することができる。また、半導体ウェハのダイシングエリアに測定用電圧を印加し

ているので、半導体チップの特性に悪影響を及ぼすことがない。

【図面の簡単な説明】

【図１】本発明の実施形態例を示す図であって、（Ａ）はウェハの平面図、（Ｂ）はＡ－Ａ線に沿う断面図である。

【図２】同実施形態例の研磨パッドの電極配置を示す平面図である。

【図３】同実施形態例で研磨した場合の電極間の静電容量を示す図である。

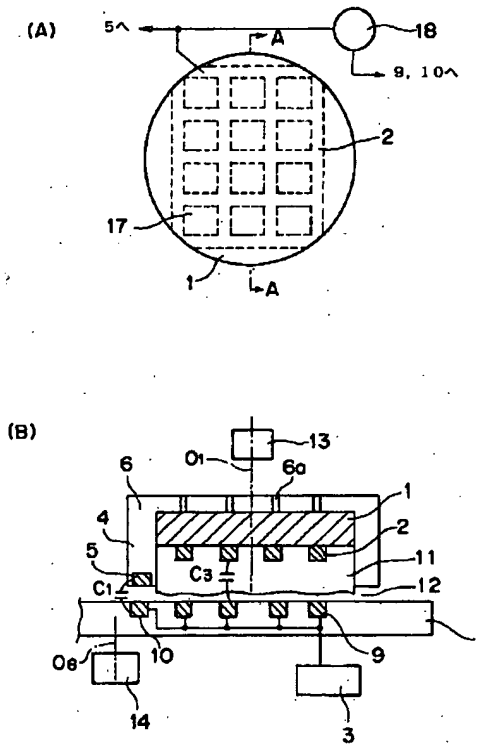
【図４】同実施形態例で研磨した場合における局所加圧を示す図であって、（Ａ）は断面図、（Ｂ）は平面図である。

【図５】従来の研磨量制御装置の概略構成図である。　＊

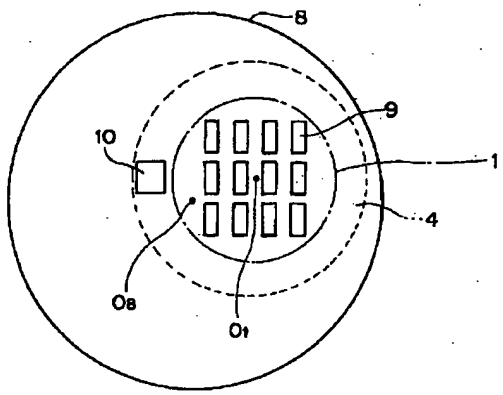
＊【符号の説明】

１　ウェハ（被研磨物）
２　電極（第１電極）
３　静電容量測定器（容量測定手段）
４　リテーナ
５　校正電極（基準電極）
６　ウェハ保持部材
６ａ　局所加圧孔（押圧手段，空気圧供給手段）
８　研磨パッド
９　測定電極（第２電極）
１０　校正用測定電極（測定用基準電極）
１１　層間絶縁膜（被研磨物）
１２　スラリ（研磨剤）
１７　チップエリア

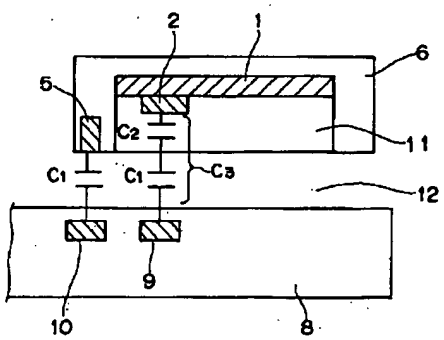
【図１】



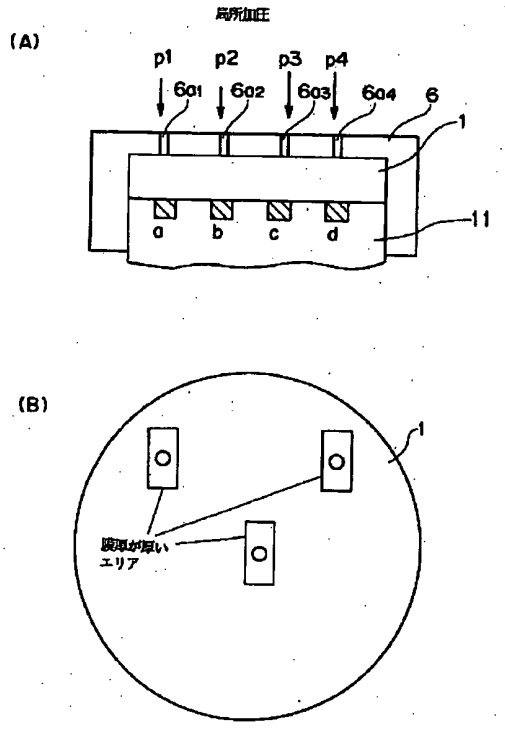
【図２】



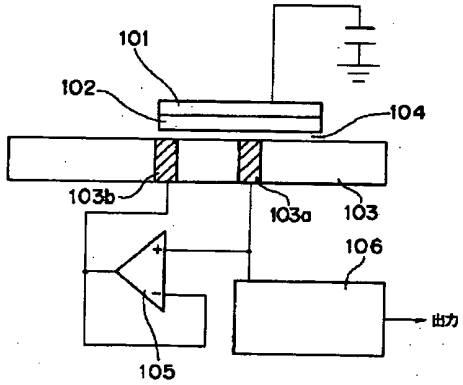
【図３】



【図４】


(A)
局所加圧
p1
p2
p3
p4
6a1
6a2
6a3
6a4
6
1
11
a
b
c
d
(B)
1
膜厚が厚い
エリア

【図５】


101
102
104
103b
103a
103
106
出力
105